PMX1
Preliminary Data Sheet

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1 FEATURES

- PowerVR II arcade performance 3D
  - Full triangle setup (hidden surface removal, shading and texturing)
  - Translucency sorting
  - RGB gouraud shading and specular highlights
  - Bilinear, trilinear and anisotropic texture filtering
  - Colour key and Alpha blended textures
  - Table and vertex fog
  - Texture compression
- 64-bit GUI accelerator
  - 3 operand ROPs
  - Hardware clipping
  - Colour expansion
  - Transparent and stretch BitBLT
- AGP 1.0 / PCI 2.1 bus master
  - DMA bus mastering for minimum CPU load
  - AGP 2x with SBA for host based textures
- TV Output
  - Fully integrated TV encoder and DAC
  - CVBS, YC and RGBS outputs
  - PAL and NTSC
  - Flicker filter
- Integrated VGA controller
- Video playback & MPEG2 decode acceleration
  - X, Y interpolated scaling
  - YUV to RGB conversion
  - Motion compensation
  - Multiple overlay windows
  - Color Key
- SGRAM/SDRAM 64-bit interface
  - Single memory for frame buffer, video and texture memory
  - 100MHz operation 800MB/s
- VMI video port
  - VMI 1.4 video port for MPEG2 decode, TV Tuner, videoconferencing
  - VBI data capture for Intercast, Closed Caption and Teletext
- Integrated 220MHz palette DAC and clock synthesiser
  - 1600x1200 resolution at 75Hz
  - True color modes up to 1024x768
- PC'98 compliant

2 OVERVIEW

PMX1 is the first integrated 2D/3D accelerator based on second generation PowerVR™ technology which extends the 3D leadership of the PowerVR™ family of chips by including high performance 2D and video processing capabilities.

PMX1 is designed to provide the highest Direct3D performance at consumer price points along with excellent 2D performance and video playback and decode acceleration.

PMX1 integrates a 3D engine, 2D engine, 24-bpp palette RAMDAC, clock generators, a VMI video input bus and TV encoder output into a 500-pin T-BGA package.

2.1 Software Drivers Support

	Windows 95	Windows 98	Windows NT4.0
Display Driver	Y	Y	Y
DirectDraw	Y	Y	Y
Direct3D	Y	Y	Y
SGL Direct II	Y	Y	Y
Video Capture		Y	
OpenGL	Y	Y	Y

Table 1. OS Feature Support

2.2 BIOS Support

Fully IBM VGA compatible BIOS

- VBE v2.0 support
- DPMS and DDC2B

2.3 Utilities

- Manufacturing test software
- OEM BIOS configuration
- Video input, graphics and TV output setup utilities

2.4 Localisation

- English
- French
- Italian
- Japanese
- German
- Spanish

3 PACKAGE INFORMATION

PMX1 is available in a 500 pin T-BGA.

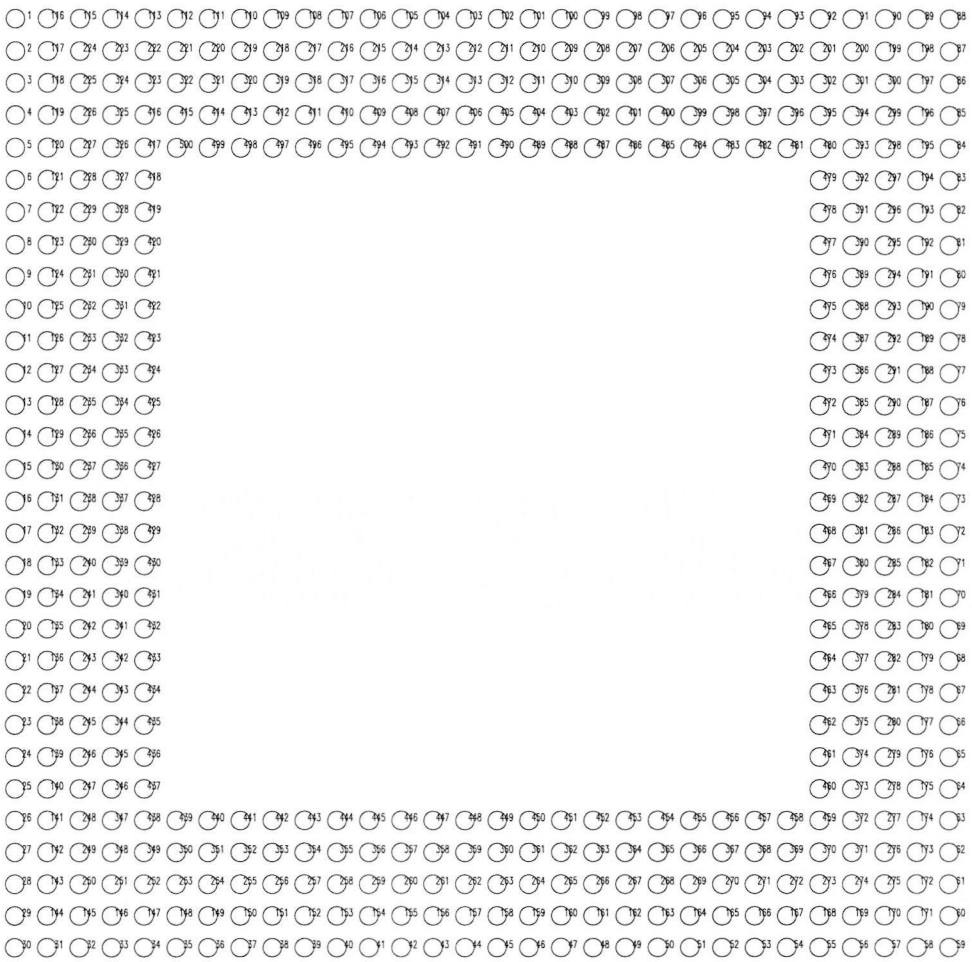


Figure 1. 500-pin TBGA Package (Top View)

3.1 Pin Descriptions

3.1.1 AGP

Name	Type	Description
AGP_ST[2:0]	I	AGP Status bus. Provides information from the arbiter to PMX1 on what it may do. ST[2:0] only have meaning to PMX1 when GNT# is asserted. Refer to AGP v.1.0 specification for more detailed decode information.
AGP_RBF#	O	Read Buffer Full indicates if PMX1 is ready to accept previously requested low priority read data or not. When asserted, the arbiter is not allowed to initiate the return of low priority read data to PMX1.
AGP_SBA[7:0]	O	Side-band address bus. Provides a dedicated bus to pass address and command to the target from the PMX master.
AGP_PIPE#	O	Pipelined Request. This is asserted by the PMX master to indicate a full-width request is to be enqueued by the target.
AGP_SB_STB	O	Side-band strobe provides timing for the AGP_SBA[7:0] bus.
AGP_AD_STB[1:0]	B	AD bus strobes. AD_STB0 provides timing for the 2x data transfer mode on the AD[15:0] bus. AD_STB1 provides timing for the 2x data transfer mode on the AD{31:16] bus. The agent which is providing the data drives these signals.
AGP_CLK133	I	This is the input pin for the AGP PLL. It should connected to the 66MHz AGP clock.
AGP_REF	I	Voltage Reference. This reference voltage is required if differential input receivers are used to achieve the tighter timing tolerances required for 133Mhz operation. It should be set to 0.4 Vddq.

3.1.2 PCI/AGP

Name	Type	Description
AGP_GNT#	I	Grant. When asserted, this signal indicates that PMX has been granted control of the PCI/AGP bus to enable the start of a bus transaction.
AGP_AD[31:0]	B	PCI/AGP multiplexed Address/Data Bus.
AGP_CBE[3:0]	B	Bus command/byte enables. For PCI, these carry the bus command during the address phase and the byte enables during the data phase. For AGP, they carry command information from the PMX master when requests are being enqueued using PIPE# and they also carry valid byte information during AGP write operations.
AGP_IDSEL	I	Initialisation Device select - chip select for PCI configuration register reads/writes.
AGP_FRAME#	B	Cycle Frame. This is asserted by the bus master to indicate the start of a PCI bus transaction. It is deasserted during the final data phase.

Name	Type	Description
AGP_IRDY#	B	Initiator ready. For PCI, a bus data phase is complete when both IRDY# and TRDY# are asserted on the same cycle. For AGP the assertion of IRDY# indicates that the PMX is ready to provide all write data for the current transaction (the master is not allowed to insert wait states). For reads, the assertion of IRDY# means that the PMX master is ready to transfer a subsequent block of data. The master is never allowed to insert a wait state during the initial block of a read transaction, however, it can do so after each subsequent block.
AGP_TRDY#	B	Target Ready. For PCI, a bus data phase is complete when both IRDY# and TRDY# are asserted on the same cycle. For AGP TRDY# indicates that the target is ready to provide read data for the entire transaction (if it takes less than 4 clock cycles), or is ready to transfer a block of data (when the transfer requires more than 4 clocks to complete)
AGP_STOP#	B	Stop - indicates PCI target disconnect
AGP_DEVSEL#	B	Device select. PMX drives this active when it decodes its address as the target for the current PCI access
AGP_PAR	B	Parity. PMX asserts this signal to verify even parity during reads on PCI accesses.
AGP_CLK	I	PCI /AGP Clock.
AGP_REQ#	O	Bus Request. PMX asserts this signal to request access to the PCI/AGP bus.
AGP_INT#	O	Interrupt Request. Connect to INTA# on PCI/AGP connector.
AGP_RST#	I	System Reset. Resets registers and state-machines to a known state.
AGP_ANP	I	AGP/PCI pad select (1=AGP, 0=PCI)
AGP_PLL_RATIO	I	Test pin – tie to GND
AGP_INEN	I	Test pin – tie to GND
AGP_CLK_RUN	I/O	CLK_RUN#

3.1.3 Memory

PMX1 supports a 64-bit 100MHz SDRAM / SGRAM memory interface.

Name	Type	Description
SD_DQM[7:0]	O	Data Mask Enable. Each bit defines whether the corresponding data byte on the bus is valid. SD_DQM[0] corresponds to the lowest byte SD_D[7:0] and SD_DQM[7] corresponds to SD_D[63:56]. In read mode, this signal controls the memory device output. In write mode, it controls the byte mask; data is written if SD_DQM is low but not written if it is high.
SD_A[11:0]	O	Address Bus
SD_CLKO	O	Memory clock output to memory devices.
SD_CLKI	I	Memory clock external reference input. This can be instead of the internally generated memory clock.

Name	Type	Description
SDCS[3:0]#	O	Chip Select. When asserted, this starts the command input cycle.
SDCAS#	O	Memory Column Address Strobe.
SD_D[63:0]	B	64-bit Data Bus
SDDSF	O	Special Function Enable. This signal is required for special SGRAM graphics commands.
SDDIR	O	Direction control (for external buffers if required).
SDWE#	O	Memory Write Enable.
SDRAS#	O	Memory Row Address Strobe

3.1.4 ROM Interface / VMI Host port

Name	Type	Description
ROMA[14:0]	O	ROM Address bus. The low 4 bits are also used as VMI host port address bits.
ROMIO	O	ROM Input/output control. When asserted, host port IO is enabled.
ROMD[7:0]	B	ROM/Host port Data
ROMRW	O	ROM/Host port read/write
ROMOE#	O	ROM Output enable control
VMICS#	O	VMI host port chip select.
DTACK#	I	Data acknowledge - VMI host port

3.1.5 Graphics Out

Name	Type	Description
IIC2_DATA	B	I^2C Data to/from monitor.
IIC2_CLK	B	I^2C clock for above
DAC_HSYNC	O	Horizontal sync.
DAC_VSYNC	O	Vertical sync.
DAC_IOB	O	Analog Blue to monitor
DAC_IOG	O	Analog Green to monitor
DAC_IOR	O	Analog Red to monitor
DAC_COMP	I	Compensation pin – tied to AGND via 0.1uf cap.
DAC_RSET	I	Reference resistor. This pin is tied to Vdd through an external resistor and is used to control full-scale DAC current.
DAC_CLK	I	Ext. DAC clock source (optional)
DAC_DGND		DAC digital ground.
DAC_AVDD1, 2, 3		DAC analog 3.3v power.
DAC_AGND1, 2, 3		DAC analog ground.
DAC_DVDD		DAC digital 3.3v power.

Name	Type	Description
DAC_DGND		DAC digital ground.

3.1.6 TV Out

Name	Type	Description
VO_FB	O	Fast blank (SCART)
VO_BLANK	O	Blank (SCART)
VO_CSYNC	O	Composite Sync.
VO_SS0	O	Function select (SCART)
VO_SENSE	I	TV cable sense pin. Not connected on PMX1.
VO_CLK	I	Input pin for the TV Out clock reference oscillator (54Mhz).
VO_YR	O	A channel output – luma/red
VO_CVG	O	B channel output – comp video/green
VO_CB	O	C channel output – chroma/blue
VO_COMPA	I	A channel compensation pin - 0.1uf cap to analog ground.
VO_COMPB	I	B channel compensation pin - 0.1uf cap to analog ground.
VO_COMPC	I	C channel compensation pin - 0.1uf cap to analog ground.
VO_MV1	I	Reserved (connect to GND)
VO_MV2	I	Reserved (connect to GND)
VO_AVDD[2:1]		TV DAC analog power 2.5v
VO_AGND[2:1]		Analog ground

3.1.7 Video in

Name	Type	Description
IIC_DATA	B	I^2C Data to/from video decoder. Provides control between video decoder & PMX.
IIC_CLK	B	I^2C clock for above.
VID_HREF	I	Horizontal reference. Indicates the start of a new line of input video.
VID_VREF	I	Vertical reference/sync. Indicates the beginning of a new field of video.
VID_YUV[7:0]	I	Video data bus.
VID_CLK	I	Video clock. Provides timing for video input data.
VID_VALID	I	Video valid. Indicates when a valid pixel is being sent.

3.1.8 System Clocks/References

Name	Type	Description
CORE_CLK	I	Core clock. This pin allows an optional core clock source to fed to the PMX1 chip as opposed to the internal core clock which is generated from REFCLK.
REF_CLK	I	Reference clock oscillator input pin. (14.318Mhz)

3.1.9 Power and Grounds

The power pins on PMX1 are connected differently according to whether PMX1 is to interface to a PCI or an AGP bus.

Name	Type	Description
3.3v VDD		3.3V I/O Supply
2.5v VDD		2.5V Core Supply
VDD5V		5V for PCI bus interface or 3.3V for AGP interface (powered from bus)
3.3v AGPVDD		3.3V for AGP interface (powered from bus) or 3.3V for PCI interface
GND		Digital Ground

3.1.10 Power on Strapping

The SGRAM/SDRAM interface also used for power-on initialisation of the configuration registers listed in table 3.1 below. Internal pull-up resistors are included internally to PMX1, therefore only pull-down resistors need fitting if required i.e., the default (no-fit) state on each pin is '1'.

Pin	Pin No.	Level	Description
SD_D[0]	81	1	AGP interface is enabled
		0	AGP interface is disabled
SD_D[1]	80	1	VGA core is enabled
		0	VGA core is disabled
SD_D[2]	292	1	DAC uses an external clock (DAC_CLK pin 100)
		0	DAC uses the clock from the internal PLL
SD_D[3]	79	1	Core uses an external clock (CORE_CLK pin 109)
		0	Core uses the clock from the internal PLL
SD_D[4]	78	1	VGA BIOS hard decode enabled
		0	VGA BIOS hard decode disabled

3.2 Pin Numbers

The following table lists the PMX1 pin-out.

Pin No.	Pin Name
1	AGP_REF
2	AGP_RST
3	AGP_GNT#
4	AGP_ST1
5	AGP_ST2
6	AGP_RBF
7	AGP_SBA3
8	AGP_SB_STB
9	AGP_SBA4
10	AGP_AD30
11	AGP_AD28
12	AGP_AD27
13	AGP_AD_STB1
14	AGP_IDSEL
15	AGP_AD21
16	AGP_AD18
17	AGP_CBE2
19	AGP_STOP
20	AGP_PAR
21	AGP_AD13
22	AGP_AD11
23	AGP_AD9
24	AGP_AD8
25	AGP_AD7
26	AGP_AD4
27	AGND_PCI
28	AGP_AD0
29	AGP_AD1
30	ROM_D6
31	ROM_D4
32	ROM_D3

Pin No.	Pin Name
33	ROM_D1
34	ROM_D0
35	ROM_A0
36	ROM_OE
37	ROM_A11
38	ROM_A9
39	ROM_A5
40	ROM_A14
41	VMICS#
42	SD_D63
44	SD_D49
45	SD_D50
46	SD_D52
47	SD_D53
48	SD_D55
49	SD_DQM7
50	SD_D33
51	SD_D34
52	SD_D43
53	SD_D42
54	SD_D38
55	SD_D39
56	SD_CLKO
57	SD_A0
58	SD_A2
59	SD_A3
60	SD_A4
61	SD_A5
62	SD_A7
63	SD_A10
64	SD_CS0

Pin No.	Pin Name
65	SD_CS3
66	SDRAS
67	SDWE
68	SD_DQM3
69	SD_D23
70	SD_D25
71	SD_D26
73	SD_D18
74	SD_D16
75	SD_DQM1
76	SD_D7
77	SD_D6
78	SD_D4
79	SD_D3
80	SD_D1
81	SD_D0
83	VID_YUV7
84	VID_YUV5
85	VID_YUV3
86	VID_YUV1
87	VID_YUV0
90	VO_AVDD2
91	VO_CBPB
92	N/C
94	VO_CLK
95	VO_CSYNC
96	VO_SENSE
97	VO_FB
98	IIC2_DATA
99	IIC2_CLK
100	DAC_CLK

Pin No.	Pin Name
101	DAC_AVDD3
102	DAC_IOR
103	DAC_IOG
104	DAC_IOB
105	DAC_HSYNC
106	DAC_VSYNC
107	PLL1_DGND
108	REF_CLK
109	CORE_CLK
110	AGP_ANP
111	AGP_INEN
113	PLL2_AVDD
114	PLL3_DGND
117	AGP_INT
118	AGP_CLK
119	AGP_INT
121	AGP_PIPE
122	AGP_SBA0
123	AGP_SBA2
124	AGP_SBA5
125	AGP_SBA6
126	AGP_AD31
127	AGP_AD26
128	AGP_AD25
129	AGP_CBE3
130	AGP_AD22
131	AGP_AD19
132	AGP_AD16
133	AGP_IRDY
134	AGP_DEVSEL
135	AGP_CLK_RUN
136	AGP_CBE1
137	AGP_AD14
138	AGP_AD12
139	AGP_CBE0

Pin No.	Pin Name
140	AGP_AD6
142	AGP_AD5
143	AGP_AD3
144	ROM_D5
146	ROM_D2
147	ROM_D7
148	ROM_IO
149	ROM_A1
150	ROM_A2
151	ROM_A3
152	ROM_A8
153	ROM_A6
154	ROM_A12
155	DTACK#
156	SD_D48
157	SD_D61
158	SD_D60
159	SD_D58
160	SD_D47
161	SD_DQM6
162	SD_D47
163	SD_D45
164	SD_D44
165	SD_D36
166	SD_D37
167	SD_D40
168	SD_DQM4
169	SD_CLKI
170	SD_A1
173	SD_A6
174	SD_A9
175	SD_A11
176	SDCS2
177	SDDSF
178	SDCAS

Pin No.	Pin Name
179	SD_DQM2
180	SD_D24
181	SD_D21
182	SD_D20
183	SD_D28
184	SD_D29
185	SD_D31
186	SD_DQM0
187	SD_D8
188	SD_D9
189	SD_D11
190	SD_D12
191	SD_D14
192	SD_D15
193	VID_HREF
194	VID_VREF
195	VID_YUV6
196	VID_VALID
197	VID_YUV7
200	VO_CBPA
201	N/C
202	N/C
203	IIC_CLK
204	IIC_DATA
205	VO_SS0
206	VO_BLANK
207	VO_MV1
208	VO_MV2
210	DAC_DVDD
211	DAC_AGND3
212	DAC_REF
213	DAC_DGND
216	PLL1_AGND
217	N/C
218	N/C

Pin No.	Pin Name
219	AGP_PLL_RATIO
221	PLL2_AGND
223	PLL3_DVDD
225	AGP_CLK133
227	AGP_ST0
229	AGP_SBA1
232	AGP_SBA7
234	AGP_AD29
235	AGP_AD24
237	AGP_AD23
238	AGP_AD20
239	AGP_AD17
240	AGP_FRAME
241	AGP_TRDY
243	AGP_AD15
246	AGP_AD10
254	ROM_A10
257	ROM_A4
258	ROM_A13
259	ROM_A7
260	ROM_RW
261	SD_D62
262	SD_D51
263	SD_D59

Pin No.	Pin Name
264	SD_D54
265	SD_D56
266	SD_D32
267	SD_D46
268	SD_D35
271	SD_D41
273	SD_DQM5
277	SD_A8
279	SDCS1
282	SD_DIR
283	SD_D22
284	SD_D27
285	SD_D19
286	SD_D17
287	SD_D30
290	SD_D5
291	SD_D10
292	SD_D2
293	SD_D13
297	VID_CLK
299	VID_YUV4
302	N/C
303	VO_CBPC
304	VO_AGND2

Pin No.	Pin Name
311	N/C
312	DAC_AGND2
313	DAC_COMP
314	N/C
317	PLL1_AVDD
321	PLL2_DGND
323	PLL3_AVDD
346	AGP_AD_STB0
395	VO_AVDD1
396	VO_VOA
397	VO_VOC
405	DAC_AVDD2
406	DAC_AVDD1
410	PLL1_DVDD
414	PLL2_DVDD
415	PLL3_AGND
481	N/C
482	VO_VOB
483	VO_AGND1
490	DAC_RSET
491	DAC_AGND1

82, 89, 93, 112, 116, 145, 171, 172, 198, 199, 209, 214, 220, 222, 224, 228, 230, 244, 245, 247, 248, 250, 252, 253, 255, 270, 272, 275, 280, 289, 295, 296, 300, 305, 307, 309, 310, 316, 318, 320, 322, 326, 327, 330, 337, 347, 349, 351, 353, 366, 370, 372, 373, 376, 383, 389, 391, 392, 393, 399, 412, 416, 417, 419, 420, 422, 423, 424, 425, 426, 427, 429, 430, 431, 432, 433, 435, 436, 438, 440, 441, 443, 444, 445, 446, 447, 448, 449, 450, 451, 452, 453, 454, 456, 457, 459, 461, 462, 464, 465, 466, 467, 468, 469, 471, 473, 474, 475, 477, 478, 480, 485, 486, 487, 488, 489, 492, 493, 494, 495, 496, 498, 499	Digital Ground

115, 215, 251, 256, 269, 274, 276, 278, 281, 288, 294, 298, 301, 306, 308, 315, 319, 324, 325, 329, 331, 333, 335, 338, 340, 342, 344, 348, 350, 352, 354, 356, 358, 359, 361, 363, 365, 367, 369, 371, 375, 377, 379, 381, 382, 384, 385, 386, 388, 390, 394, 398, 400, 402, 404, 407, 409, 411, 413	2.5v
43, 72, 88, 355, 357, 360, 362, 364, 368, 374, 378, 380, 387, 401, 403, 408, 439, 442, 455, 458, 460, 463, 470, 472, 476, 479, 484, 497	3.3v VDD
236, 328, 332, 339, 341, 345, 418, 421, 428, 434, 437, 500	3.3v AGPVDD (AGP) or 3.3v VDD (PCI)
18, 120, 141, 226, 231, 233, 242, 249, 334, 336, 343.	5v (PCI) or 3.3v AGPVDD (AGP)

4 FUNCTIONAL DESCRIPTION

4.1 General

PMX1 is a single chip multimedia display device which integrates 2D and 3D accelerators with separate palette DAC and clock synthesisers for graphics and TV output including a digital video encoder.

PMX1 includes glue-less interfaces to AGP/PCI, SDRAM/SGRAM and a VMI video port.

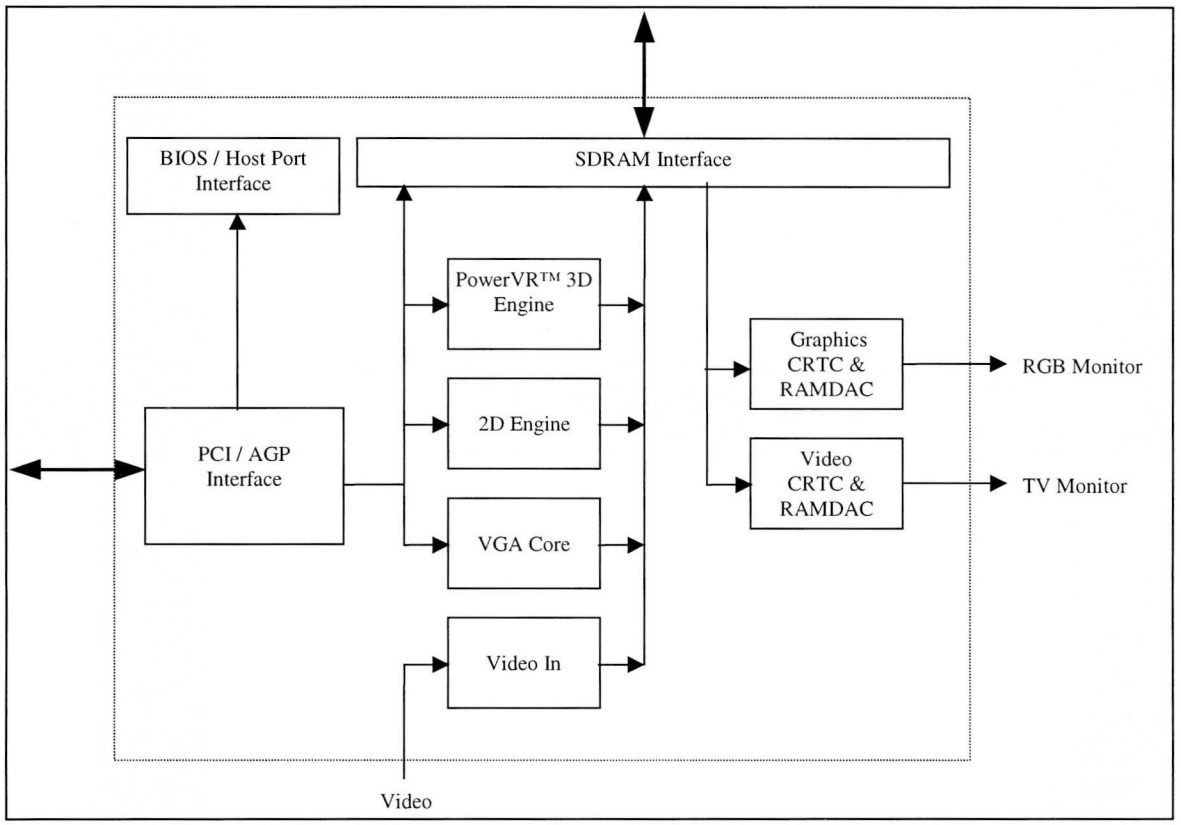


Figure 2. PMX1 Simplified Block Diagram

4.2 Host Interface

The PMX1 host interface is a glue-less PCI v2.1 (66MHz) and AGP v1.0 interface which acts as a bus master for 2D and 3D parameters as well as host based textures and video capture.

The PCI interface supports Memory Read, Memory Write, IORead, IOWrite, Memory Read Line, Memory Read Multiple, and Memory Write Multiple commands, and has full logical to physical mapping support.

The AGP interface is a full 2x with side band addressing implementation supporting a peak bandwidth of 530MB/S. It's read queue buffer supports 32 outstanding commands.

PMX1 incorporates a page translation table allowing for bus mastering of scattered data to and from host memory.

PCI power management device states of D0, D1, D2, $D3_{HOT}$ and $D3_{COLD}$ are implemented allowing ACPI compliant system design.

Sub System Vendor ID is also supported in the PCI configuration space.

4.3 Memory Interface

PMX1 is designed with a 64-bit 100MHz SDRAM / SGRAM memory interface with a peak bandwidth of 800MB/S. On-chip caches and memory controller ensures that bandwidth is shared efficiently between the 2D, 3D and display functions.

Between 4MB and 16MB of SDRAM or SGRAM can be supported as shown below.

Memory Type	Number of devices	Memory
16 Mbit SDRAM	4	8MB
	8	16MB
8 Mbit SGRAM	4	4MB
	8	8MB
16 Mbit SGRAM	2	4MB
	4	8MB
	8	16MB

Table 2. PMX1 Memory Configurations

4.4 2D Graphics Engine

PMX1 incorporates a powerful 2D graphics accelerator which accelerates all the three operand ROP BitBLTs, Transparent BLTs and Blend BLTs as well as allowing video scaling and color space conversion in a single pass function. The engine has been optimised to ensure there is no penalty for operating in 24bpp packed pixel modes. Other 2D operations supported in hardware include clipping, mono to colour expansion, points and lines.

The engine bus masters both it's commands and parameters from either framebuffer or host which allows the CPU to do the minimum amount of work, increasing system throughput and enabling the use of Write Combining.

4.4.1 VGA Core

A separate, independent VGA core is included in PMX1. This is fully IBM VGA compliant and supports all standard VGA modes.

4.5 3D Graphics Engine

PMX1 uses the 2nd generation PowerVR 3D core to provide the huge performance and advanced features required by tomorrow's 3D applications.

The PowerVR 3D engine is a display list renderer which takes a whole scene of data to be rendered, partitions the data into screen tiles, performs hidden surface removal (without the need of a Z-buffer) and performs deferred texturing on the resultant visible pixels.

Performance is ensured by the inclusion of complete hardware set-up of both triangle and texturing / shading parameters, the scene parameters being stored in host memory and bus mastered by PMX1 for maximum performance.

PowerVR supports Z-buffer-less hidden surface removal, RGB gouraud shading, perspective correct texture mapping, alpha blending and advanced texture filtering including bilinear, trilinear and anisotropic filtering.

4.6 Graphics Output

The graphics pipeline incorporates color space conversion, overlay support, scaling and LUT. It can read pixel data in both RGB and YUV422 formats and performs Gamma correction (through the LUT). DPMS and DDC2B are supported.

4.7 TV Output

PMX1 can output NTSC and PAL encoded images as a composite, YC or RGB signal which is entirely independent of the main graphics display. The TV Output also supports overscan and underscan control, flicker filtering and Macrovision copy protection.

4.8 Video Input

A VMI 1.4 interface allows capture of video data at up to 70MB/s data rates, including support for cropping, VBI capture, bus mastered data capture and image decimation.

4.9 BIOS / VMI Host Port

PMX1 shares the BIOS interface with a VMI Host port used to interface to external devices such as MPEG2 decoders.

5 Mode Support

5.1 Graphics Output

Resolution	Colours	Refresh
1600x1200	256	60, 72, 75
1280x1024	256	60, 72, 75, 100
1152x864	256 65 thousand	60, 72, 75, 100 60, 72, 75
1024x768	256 65 thousand 16.7 million	60, 72, 75, 100 60, 72, 75, 90 60, 72, 75
800x600	256 65 thousand 16.7 million	60, 72, 75, 100 60, 72, 75, 100 60, 72, 75, 90
640x480	256 65 thousand 16.7 million	60, 72, 75, 100 60, 72, 75, 100 60, 72, 75, 100
VGA Modes 0,1,2,3,4,5,6,7,0Dh, 0Eh, 0Fh, 10h, 11h, 12h, 13h		

5.2 TV Output

Standard	Resolution	Colours	Refresh
PAL	716x576 / 640x480 / 800x600	256 / 65 thousand / 16.7 million	50
NTSC	712x480 / 640x480 / 800x600	256 / 65 thousand / 16.7 million	60

6 ELECTRICAL SPECIFICATIONS

6.1 Absolute Maximum Ratings

Parameters	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD		3.6	V
Input/Output voltage	VI/VO	2.5V interface	3.6	V
		3.3V interface	4.6	V
		5V interface	xx	V
Latch-up current	I_{LATCH}		1	A
Operating temperature	TOPT		-40 to +85	°C
Storage temperature	TSTG		-65 to +150	°C

6.2 Recommended Operating Conditions

Parameters	Symbol	2.5V Buffer		3.3V Buffer		Unit
		MIN	MAX	MIN	MAX	
Power Supply Voltage	VDD	2.3	2.7	3.0	3.6	V
High level input voltage	VIH	1.7	VDD+ 0.3	0.5 VDD	VDD+ 0.5	V
Low level input voltage	VIL	-0.3	0.7	-0.5	0.3 VDD	V

6.3 PCI Bus Timing

Parameters	Symbol	Condition	Spec.		Sim.		
			Min.	Max.	Min	Typ	Max
Output rise slew rate	slewr	0.4V to 2.4V load	1	5	1.14		4.92
Output fall slew rate	slewf	2.4V to 0.4V load	1	5	1.32		4.27
Switching Current High	Ioh(AC)	0< Vout<=1.4V	-44	-	-62.5	-	-
		Vout = 3.1V	-	-142	-	-	-45.4
Switching Low	Iol (AC)	Vout.>=2.2V	95	-	132.2	-	-
		Vout =0.71V	-	206	-	-	180

6.4 AGP Bus Timing

TBD

6.5 SDRAM Interface Timing

PMX has the following internal clock architecture.

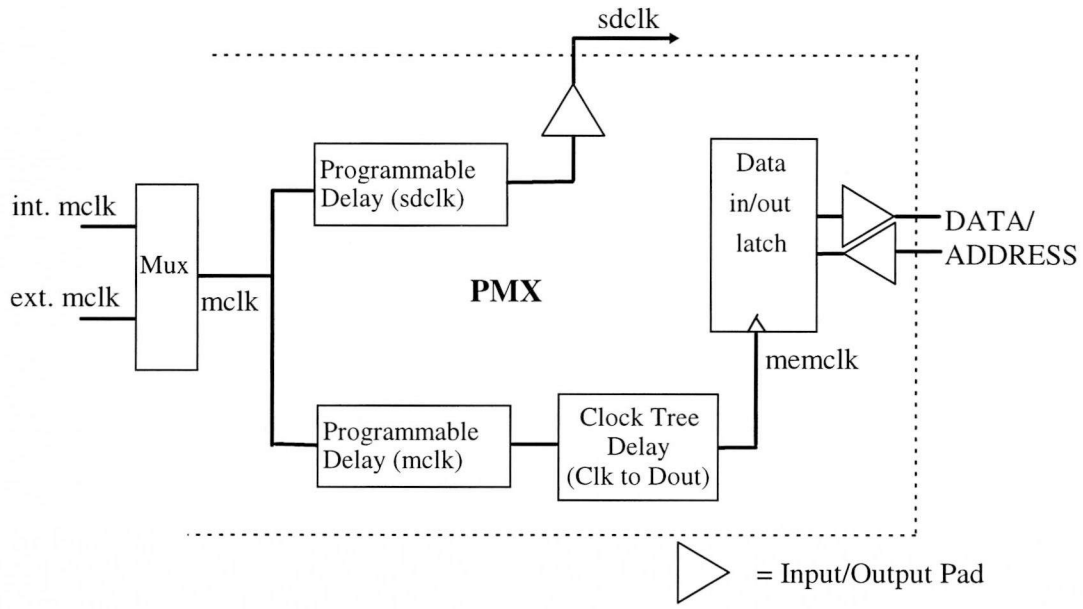


Figure 3. Simplified PMX Memory Stage Architecture

The various elements have the following timing characteristics:

Name	Min	Max	Typ	Notes
Pad Delay			1.5nS	
MCLK to SDCLK	TBD nS	TBD nS	TBD nS	Programmable Delay
MCLK to MEMCLK		TBD nS	TBD nS	Programmable Delay
CLK to D_{out}	TBD nS	TBD nS		Programmable Delay + tree delay
Data in setup t_{PSU}	0.5nS			
Data in hold t_{PH}	1.5nS			
Data/add out delay t_{PAC}	2.5nS			Ref. to memclk (incl. pad delay)

Then for -10nS SDRAM devices with the following timings:

Name	Min	Max	Typ	Notes
Data/addr input setup t_{SDSU}	2.5nS			
Data/addr input hold t_{SDH}	1nS			
Access time t_{AC}		8nS		
Data output hold t_{OH}	4nS			

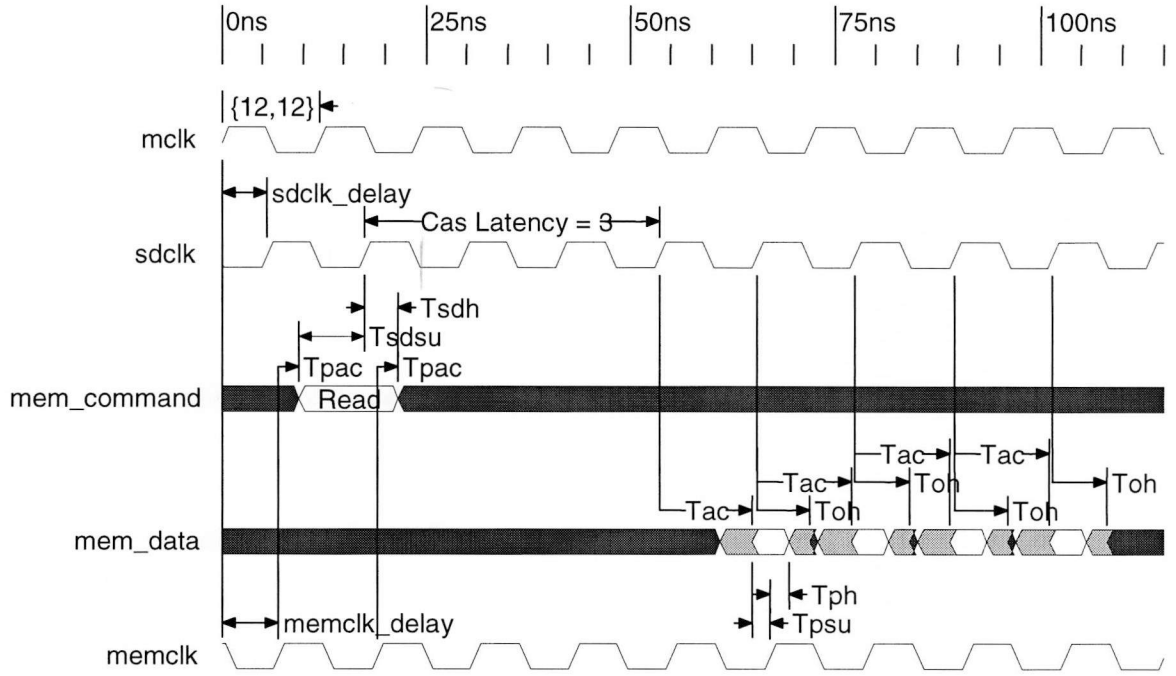


Figure 4. SDRAM Timing

6.6 BIOS/VMI Host port Timing

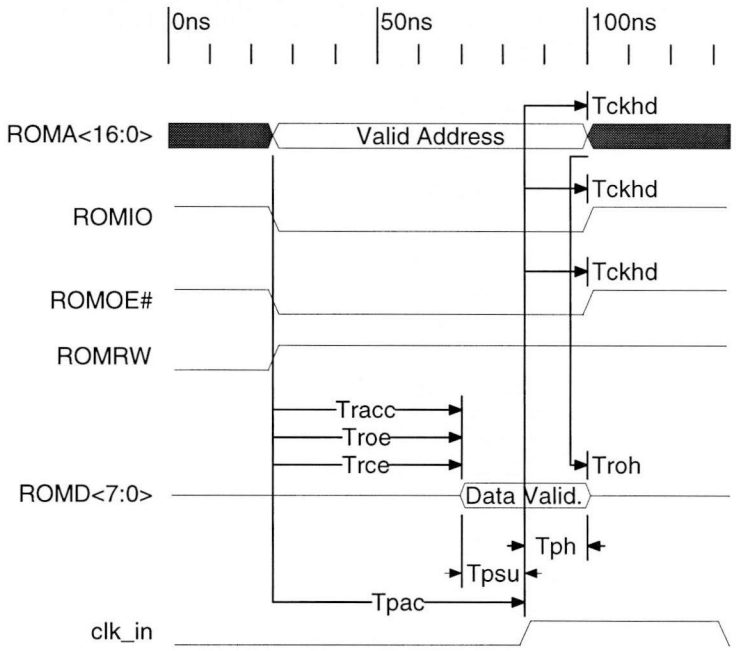
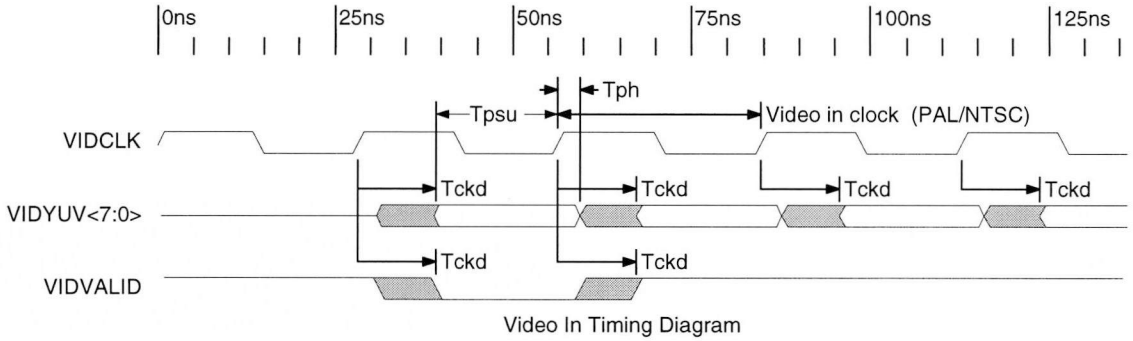


Figure 5. ROM Interface Read Timing

Read operation timing characteristics with 45nS devices:

Name	Min	Max	Typ	Notes
ROM access tRACC, tRCE		45ns		for 45ns part
ROM access from OE# tROE		25ns		for 45ns part
ROM data out hold tROH		0ns		for 45ns part
PMX data-in latch delay from commence of access tPAC	15ns	240ns		Programmable for ROM part in steps of approx 15ns (coreclk frequency)
Control signal hold time after latch tCKHD			15ns	1 x coreclk delay
Data in setup tPSU	0.5nS			for PMX1
Data in hold tPH	1.5nS			for PMX1

6.7 VMI Video Timing



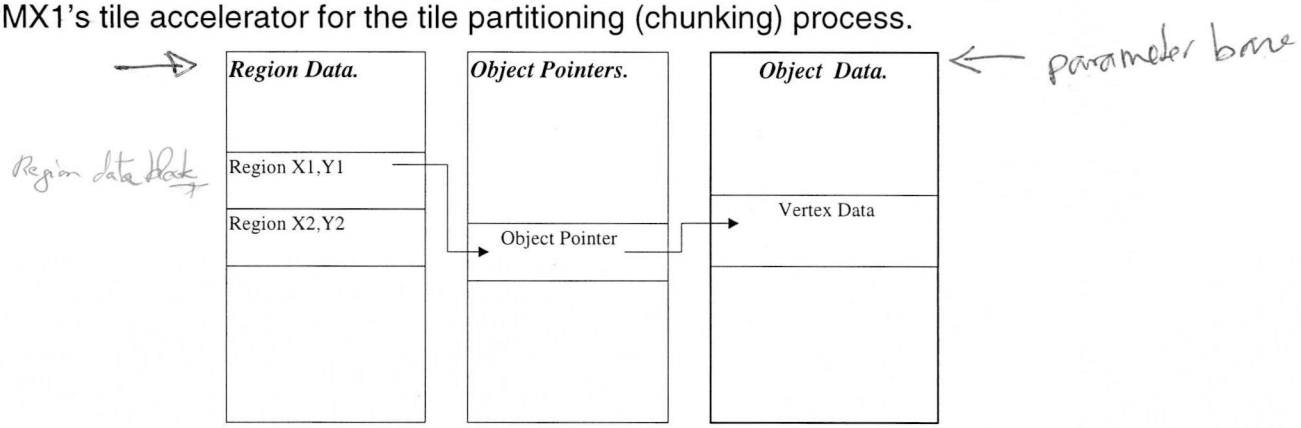
Video In Timing Diagram

Figure 6. Video Interface Timing

Name	Min	Max	Typ	Notes
Vidclk to data/control delay tCKd.	3ns	11ns		Bt829a
Data in setup tPSU	0.5nS			PMX1
Data in hold tPH	1.5nS			PMX1
VIDCLK frequency			28.63Mhz 35.47Mhz	NTSC PAL

APPENDIX A. 3D DATA FORMAT

This section describes the 3D scene data format for PMX1. The data format described is created by a driver (e.g. Direct3D HAL, SGL DirectII) which uses PMX1's tile accelerator for the tile partitioning (chunking) process.



Region Data

A Region Data block points to the start of a list of pointers to Objects that are potentially visible in that Region. Each Region Data block consists of five 32 bit words, containing a header word and 4 pointers as follows:-

Bit 31	*30*	*29*	*28*	*27-14*	*13-8*	*7-2*	*1-0*
Last Region	Keep Z State	PreSort	Flush Acc Buffer	Reserved	Region Y Position (*16)	Region X Position (*32)	Reserved
Opaque List Pointer							
Opaque Modifier Volume List Pointer							
Translucent List Pointer							
Translucent Modifier Volume List Pointer							

Last Region

This marks the end of the rendering region data. It must be set on the last region.

Keep Z State

If this bit is cleared the state of the Z buffer is reset. If set the Z state of the ISP is not retained.

PreSort

When cleared, translucency auto sorting is used and when set it is not, requiring that the driver provides it with pre sorted translucent objects.

Flush Accumulation Buffer

Setting this bit flushes the blend accumulation buffer prior to processing the tile region. Otherwise the state is retained.

Region Y & X Position

This specifies the top left pixel of the region. The supplied Y and X values are multiplied by 16 and 32 respectively.

List Pointer fields

The format of each of the four list pointers is as follows:

Bit 31	*30-28*	*27-2*	*1-0*
Empty PTR	Reserved	Pointer to Object List (32 bit resolution)	00

These list pointers point to the start of a block of Object Pointers.

An empty list will be identified by a '1' in the Empty PTR field. Note, if this bit is set, then all other bits in the pointer are irrelevant.

Object Pointers.

The object pointers are used to describe which objects in a particular region.

Triangle Strip

Bits 31	*30-25*						*24*	*23-21*	*20-0*
0	Mask						Shadow	Skip	Triangle Strip Start (32bit Word Address)
	T0	T1	T2	T3	T4	T5			

Mask field.

The 6 bit mask allows any combination of triangles in a strip to be added to a region. For example if 'T0' and 'T3' are set, then the first and fourth triangles in the strip are visible in that region.

Shadow Bit.

The Shadow bit communicates that the surface has inside/outside information attached. In 'Intensity Volume Mode', this bit describes whether the surface accepts a shadow.

Skip Field.

The Skip field communicates the size of a vertex, so random access into the strip is possible.

If the Shadow bit is not set, then the size of a vertex is 'Skip + 3' words long. If the Shadow bit is set and PMX1 is in 'Parameter Selection Volume Mode' , then the size of a vertex is 'Skip*2 +3' words long.

Object Pointer Block Link

Bits 31-29	*28*	*27-2*	*1-0*
111	End of List	Next Pointer Block (32bit Word Address)	00

The link pointer either redirects where pointers should be fetched from, or communicates that the end of list has been reached.

Parameter Formats

What follows is the complete list of 3D parameter formats that supported by PMX1. Note that all objects may be represented by two forms, one which uses X, Y and 1/W to describe a vertices position and a second which uses X, Y, Z and 1/W. In the second case Z is used for depth sorting and 1/W is used for texturing calculations. Which vertex format is used is determined by a global register.

The format where only 1/W is used requires 1 less DWORD of space per vertex in each case than the format which specifies both Z and 1/W.

In each format the vertex data (shown in grey) may be repeated between 2 and 7 times in order to represent triangle strips between 1 and 6 faces in length.

Shadow Triangle

	Format #1
0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word (ignored)
0x08	Texture Control Word (ignored)
0x0c	X
0x10	Y
0x14	1/W

Format #2	
ISP/TSP Instruction Word	0x00
TSP Instruction Word (ignored)	0x04
Texture Control Word (ignored)	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18

Gouraud Shaded Triangle (No Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word (ignored)
0x0c	X
0x10	Y
0x14	1/W
0x18	Base Colour

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word (ignored)	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
Base Colour	0x1C

Gouraud Shaded Triangle (Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word (ignored)
0x0c	X
0x10	Y
0x14	1/W
0x18	Base Colour
0x1C	Offset Colour

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word (ignored)	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
Base Colour	0x1C
Offset Colour	0x20

16 bit UV Textured Gouraud Shaded Triangle (No Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word
0x0c	X
0x10	Y
0x14	1/W
0x18	U I V
0x1C	Base Colour

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
U I V	0x1C
Base Colour	0x20

32 bit UV Textured Gouraud Shaded Triangle (No Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word
0x0c	X
0x10	Y
0x14	1/W
0x18	U
0x1c	V
0x20	Base Colour

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
U	0x1c
V	0x20
Base Colour	0x24

16 bit Textured Gouraud Shaded Triangle (Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word
0x0c	X
0x10	Y
0x14	1/W
0x18	U I V
0x1c	Base Colour
0x20	Offset Colour

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
U I V	0x1c
Base Colour	0x20
Offset Colour	0x24

16 bit Bump Map Triangle

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word
0x0c	X
0x10	Y
0x14	1/W
0x18	U I V
0x1c	Base Colour
0x20	K1K2K3Q

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
U I V	0x1c
Base Colour	0x20
K1K2K3Q	0x24

32 bit Textured Gouraud Shaded Triangle (Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word
0x0c	X
0x10	Y

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word	0x08
X	0x0c
Y	0x10

0x14	1/W
0x18	U
0x1c	V
0x20	Base Colour
0x24	Offset Colour

Z	0x14
1/W	0x18
U	0x1c
V	0x20
Base Colour	0x24
Offset Colour	0x28

32 bit Bump Map Triangle.

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word
0x08	Texture Control Word
0x0c	X
0x10	Y
0x14	1/W
0x18	U
0x1c	V
0x20	Base Colour
0x24	K1K2K3Q

ISP/TSP Instruction Word	0x00
TSP Instruction Word	0x04
Texture Control Word	0x08
X	0x0c
Y	0x10
Z	0x14
1/W	0x18
U	0x1c
V	0x20
Base Colour	0x24
K1K2K3Q	0x28

Gouraud Shaded Triangle With Two Volumes (No Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0(ignored)
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1(ignored)
0x14	X
0x18	Y
0x1c	1/W
0x20	Base Colour 0
0x24	Base Colour 1

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0(ignored)	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1(ignored)	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
Base Colour 0	0x24
Base Colour 1	0x28

Gouraud Shaded Triangle With Two Volumes (Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0(ignored)
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1(ignored)
0x14	X
0x18	Y
0x1C	1/W

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0(ignored)	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1(ignored)	0x10
X	0x14
Y	0x18
Z	0x1C

0x20	Base Colour 0
0x24	Offset Colour 0
0x28	Base Colour 1
0x2C	Offset Colour 1

1/W	0x20
Base Colour 0	0x24
Offset Colour 0	0x28
Base Colour 1	0x2C
Offset Colour 1	0x30

16bit UV Tex Gouraud Shaded Triangle With Two Volumes (No Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1
0x14	X
0x18	Y
0x1c	1/W
0x20	U | V 0
0x24	Base Colour 0
0x28	U | V 1
0x2c	Base Colour 1

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
U | V 0	0x24
Base Colour 0	0x28
U | V 1	0x2c
Base Colour 1	0x30

32 bit UV Tex Gouraud Shaded Triangle With Two Volumes (No Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1
0x14	X
0x18	Y
0x1c	1/W
0x20	U 0
0x24	V 0
0x28	Base Colour 0
0x2c	U 1
0x30	V 1
0x34	Base Colour 1

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
U 0	0x24
V 0	0x28
Base Colour 0	0x2c
U 1	0x30
V 1	0x34
Base Colour 1	0x38

16 bit Textured Gouraud Shaded Triangle With Two Volumes (Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0	0x08

0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1
0x14	X
0x18	Y
0x1c	1/W
0x20	U I V 0
0x24	Base Colour 0
0x28	Offset Colour 0
0x2c	U I V 1
0x30	Base Colour 1
0x34	Offset Colour 1

TSP Instruction Word 1	0x0c
Texture Control Word 1	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
U I V 0	0x24
Base Colour 0	0x28
Offset Colour 0	0x2c
U I V 1	0x30
Base Colour 1	0x34
Offset Colour 1	0x38

16 bit Bump Map Triangle With Two Volumes

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1
0x14	X
0x18	Y
0x1c	1/W
0x20	U I V 0
0x24	Base Colour 0
0x28	K1K2K3Q 0
0x2c	U I V 1
0x30	Base Colour 1
0x34	K1K2K3Q 1

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
U I V 0	0x24
Base Colour 0	0x28
K1K2K3Q 0	0x2c
U I V 1	0x30
Base Colour 1	0x34
K1K2K3Q 1	0x38

32 bit Textured Gouraud Shaded Triangle With Two Volumes (Offset Colour)

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1
0x14	X
0x18	Y
0x1c	1/W
0x20	U 0
0x24	V 0
0x28	Base Colour 0

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
U 0	0x24
V 0	0x28

0x2c	Offset Colour 0
0x30	U 1
0x34	V 1
0x38	Base Colour 1
0x3c	Offset Colour 1

Base Colour 0	0x2c
Offset Colour 0	0x30
U 1	0x34
V 1	0x38
Base Colour 1	0x3c
Offset Colour 1	0x40

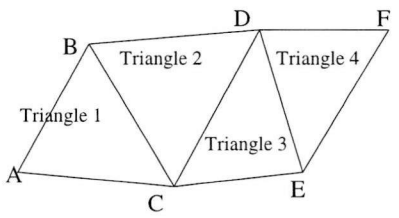
32 bit Bump Map Triangle With Two Volumes

0x00	ISP/TSP Instruction Word
0x04	TSP Instruction Word 0
0x08	Texture Control Word 0
0x0c	TSP Instruction Word 1
0x10	Texture Control Word 1
0x14	X
0x18	Y
0x1c	1/W
0x20	U 0
0x24	V 0
0x28	Base Colour 0
0x2c	K1K2K3Q 0
0x30	U 1
0x34	V 1
0x38	Base Colour 1
0x3c	K1K2K3Q 1

ISP/TSP Instruction Word	0x00
TSP Instruction Word 0	0x04
Texture Control Word 0	0x08
TSP Instruction Word 1	0x0c
Texture Control Word 1	0x10
X	0x14
Y	0x18
Z	0x1c
1/W	0x20
U 0	0x24
V 0	0x28
Base Colour 0	0x2c
K1K2K3Q 0	0x30
U 1	0x34
V 1	0x38
Base Colour 1	0x3c
K1K2K3Q 1	0x40

Vertex Order

The following diagram shows a triangle strip of length 4.



The Order that the vertices are stored is ABCDEF. Triangle1 is defined by *ABC*, Triangle 2 is defined by *CBD* (not *BCD*), Triangle 3 by *CDE*, and Triangle 4 by *EDF* (not *DEF*). This then guarantees that the ordering of the points (clockwise in this example) is consistent between all triangles.

X, Y, 1/W, Z Data

These are described in IEEE single precision floating point format. The X and Y are the screen co-ordinates of the vertex, Z refers to the vertices untransformed depth value, and 1/W to the inverse of it's perspectively projected depth value.

Colour Data

The colours are packed into 32 bits, with the following format:

Alpha (8bits)	Red (8bits)	Green (8bits)	Blue (8bits)

MSB LSB

Note 1: an Alpha of 0 will implies fully translucent, and an Alpha of 255 is fully opaque.

Note 2: The Alpha component in the Offset colour can be used as Vertex Fog.

UV Texture Coordinates

These values are described in two possible formats. If the '16 Bit UV' bit in the 'ISP/TSP Instruction Word' is clear then the UV pair are in IEEE single precision floating point format. If the '16 Bit UV' bit is set, then a UV pair is placed in one 32 bit word by taking the top 16 bits of each IEEE float. The U is stored in the most significant 16 bits, and the V is stored in the least significant 16 bits.

Coordinates outside the range 0.0 to 0.9999 will be in the Flip/Clamp/Wrap region.

Two Volumes format

If the shadow bit in the pointer is set, and 'Parameter Selection Volume Mode' has been selected, then data for two volumes will be supplied. If the surface is outside the defined volume, then the parameters with '0' appended to the name will be selected. If the surface is inside the defined volume, then the parameters with '1' appended to the name will be selected.

Bump Mapping format

The K1K2K3Q parameters are taken from the third vertex (in the same manner as flat shaded surfaces).

ISP/TSP Instruction Word

The ISP/TSP Instruction word is set out as follows:

Bits 31-29	28-27	26	25	24	23	22	21	20	19-0
Depth Compare Mode	Culling Mode	Depth Write Disable	Texture	Offset	Gouraud shading	16 Bit UV	Reserved	D Calc Control	Reserved

If the surface is in one of the Modifier Volume Lists, the word is interpreted as follows:

Bits 31-29	28-27	26-0

Volume instruction	Culling Mode	Reserved

Depth Compare Mode.

The depth compare mode in combination with the 'Depth Write Disable' field is used to support the various OpenGL and D3D style of Z-buffer updates.

Culling Mode.

To support arbitrary back-face culling, the *culling mode* field defines the following modes...

Cull mode	Code
No culling	0
Cull if Small	1
Cull if Negative	2
Cull if Positive	3

Depth Write Disable

If the *Depth Write Disable* flag is set, the depth value is not updated as a result of the depth test.

Texture Bit

This bit specifies if the surface is textured or just shaded.

Offset

If set, then the colour offset values are relevant, and must added into the shading calculation. If Gouraud shading, it must be interpolated.

Gouraud Shading

If set, the three colours associated with a triangle will have perspective correct interpolated colour across the surface. If this bit is 0, then the colour of the third vertex will be used over the whole surface.

16 bit UV

If the 'Texture' bit is set and the '16 bit UV' bit is set, then a UV pair is placed in one 32 bit word by taking the top 16 bits of each IEEE float. The U is stored in the most significant 16 bits, and the V is stored in the least significant 16 bits.

DCalc Control.

This is used to control the method of calculating 'D' (or Level Of Detail) for MIP-mapping.

Volume Instruction.

PMX1 will support inclusion and exclusion volumes constructed entirely from triangles. The type of these volumes must be identified on a per-region basis via a special instruction on the triangle.

Volume Instruction	Code
'Normal' Polygon	0
Inclusion Last Poly	1
Exclusion Last Poly	2
Reserved	3-7

The 'Last polygon' instructions indicate that this is the last polygon for a given volume in a region, while the 'normal polygon' is just one of the polygons forming the boundary of the 'current' volume.

TSP Instruction Word

The TSP Instruction word is set out as follows:

Bits 31-29	28-26	25	24	23-22	21	20	19
SRC Alpha Instr	DST Alpha Instr	SRC Select	DST Select	Fog Control	Colour Clamp	Use Alpha	Ignore Tex Alpha

Bits 18-17	Bits 16-15	14	13	12	11-8	7-6	5-3	2-0
U Mode	V Mode	PassAB	Filter Mode	Supersample Texture	MIP-Map 'D' adjust	Texture/Shading Instruction	Texture U Size	Texture V Size

SRC / DST Alpha Instructions

The accumulation buffer controls consist of two 3 bit fields which control the alpha blend functions, and a 2 bit Source/Destination Select field.

The 2 bit Source/Destination Select field controls whether the blending uses a secondary accumulation buffer which can be used for special effects such as shadow and bump maps.

The blend function assumes two RBGA values, SRC and DST, which are combined and the result put back into DST, via the following function...

```
DST :=      SRC     *     BlendFunction(SRC     Alpha     Instruction)     +
            DST * BlendFunction(DST Alpha Instruction)
```

where

```
BlendFunction(Instruction)
```

takes as input the three bit *instruction* along with the SRC and DST colours, and returns a vector of *four* alpha weighting values - one for each of RGBA. The *instruction* codes are defined as:

Instruction	Field Value	Values Returned
Zero	0	(0, 0, 0, 0)
One	1	(1, 1, 1, 1)
'Other' Colour	2	(O_R, O_G, O_B, O_A)
Inverse 'Other' Colour	3	(1 - O_R, 1- O_G, 1 – O_B, 1 - O_A)
SRC Alpha	4	(S_A, S_A, S_A, S_A)
Inverse SRC Alpha	5	(1- S_A, 1 - S_A, 1 - S_A, 1 - S_A)
DST Alpha	6	(D_A, D_A, D_A, D_A)
Inverse DST Alpha	7	(1- D_A, 1 - D_A, 1- D_A, 1 - D_A)

The 'Other Colour' and 'Inverse Other Colour' instructions mean that when the `BlendFunction` is multiplying by SRC, the colour of the DST is used and vice versa.

The addition that is performed checks for possible overflow and clamps the resulting values appropriately.

SRC / DST Select.

The actual SRC and DST values are selected by the two bit SRC-DST Select field.

If the SRC Select bit is set, then rather than using the colours output from the current surface's shading/texturing computation, PMX1 uses the contents of the secondary accumulation buffer as the source.

If the DST Select bit is set, then rather than using the colours in the primary accumulation buffer shading/texturing, PMX1 uses the contents of the secondary accumulation buffer as the Destination. This applies to all occurrences of DST in the above equation.

Fog Control

The fog field indicates the following possibilities:

Fog Mode	Bit Pattern	Description
Look Up Table	00	Use a table indexed by 1/W and piece-wise linear interpolation to generate fog 'alphas'.
Per Vertex	01	Use the 'fog alpha' in the offset colours alpha. This is interpolated if 'Gouraud' is switched on, otherwise is constant. This bit pattern should only be set if the 'Offset' bit is also set, otherwise it will default to 'No fog'.
No fog	10	Disable fogging on the current surface
Look Up Table Mode 2	11	The fog density is calculated as mode 0, but instead of interpolating the surface colour with the fog colour, the fog colour replaces the surface colour, and the density is placed in the alpha channel.

Colour Clamp

This clamps the calculated colour just before it is fogged. An Underflow and Overflow colour register is programmed by the user.

Use Alpha

If set, then the per-point alpha bits in the colour are relevant, and must be interpolated when Gouraud shading. If zero, then the alpha should be regarded as fully opaque (i.e., 1.0f or 255 in 8 bit fixed point).

Ignore Texture Alpha

If the texture has an alpha value, this allows that alpha to be ignored. In effect, if the bit is set, the alpha of the texture is assumed to be fully opaque, i.e., 1.0. Note that this *only* refers to the alpha of the texture.

U Mode & V Mode

The U Mode and V Mode bits control overflow conditions on U & V as shown in the following table:

U / V Mode	Bit Pattern	Description
Repeat	00	Texture repeats across a surface
Flip	01	U & V values above 1 'flip'. The decimal part is used either as is or as (1-Value)
Clamp	10	U & V are clamped at 0 and 1.
Wrap	11	U & V are interpolated for the shortest distance

Filter Mode

This field determines the type of basic texture filtering that will be applied as follows:

Field Values	Filter Mode
0	Point Sampled
1	Bilinear Filter

PassAB

Field Values	
0	Pass A
1	Pass B

This field determines which pass is currently being used. If it is Pass A then the texels are multiplied by the fractional (1-D), if it is Pass B they are multiplied by fractional D.

Super-Sample texture

Setting this performs super-sampling with the chosen filter mode. When MIP mapping, the hardware automatically chooses the next higher resolution MIP map level.

MIP-map D Adjust

As the MIP map '*D*' value will be calculated entirely by hardware, it may be necessary to add a 'tweak' value to forcibly make it larger or smaller to trade-off aliasing vs. blurring. The adjust value will be *multiplied* by the 'default' *D* value computed by the hardware.

The four bit unsigned value will be in a fixed point format, with 2 bits of fraction. Example values are given in the following table.

Example 'D' Adjust bit pattern	Equivalent value
00.00	*Illegal*♦
00.01	0.25
01.00	1.0
11.11	3.75

♦ Since a D value of zero is invalid, it does not make sense to multiply by zero.

Texture/Shading Instruction

This field determines how the interpolated shading values (Base Colour and alpha and Offset colour) are combined with the texture's alpha and texture.

Instruction	Field Value	Description
Decal	0	$PIX_{RGB} = TEX_{RGB} + OFFSET_{RGB}$ $PIX_A = TEX_A$
Modulate	1	Texture colour multiplied by shading colour. Texture alpha replaces shading alpha. $PIX_{RGB} = COL_{RGB} * TEX_{RGB} + OFFSET_{RGB}$ $PIX_A = TEX_A$
Decal Alpha	2	Texture colour blended with shading colour according to texture alpha. $PIX_{RGB} = (TEX_{RGB} * TEX_A) + (COL_{RGB} * (1 - TEX_A)) + OFFSET_{RGB}$ $PIX_A = COL_A$
Modulate Alpha	3	Texture colour multiplied by shading colour. Texture alpha multiplied by shading alpha. $PIX_{RGB} = COL_{RGB} * TEX_{RGB} + OFFSET_{RGB}$ $PIX_A = COL_A * TEX_A$

NOTE: This instruction is ignored if the surface is non-textured.

U Size

This field gives the U (or X dimension) of the texture as follows:-

Field Value	Dimension
0	8
1	16
2	32
3	64
4	128
5	256
6	512
7	1024

V Size

This field gives the V (or Y dimension) of the texture. It is encoded in exactly the same manner as the U Size field.

Texture Control Word

The texture control word is set out as follows:

Bit 31	30	29-27	26	25	24-23	22	21	20-0
MIP Mapped	VQ Compressed	Pixel Format	Scan Order	Stride Select	Color Key Control	MultiPass Texture Filtering	Palettised Texture	Texture Address

This word is only used when the Texture bit is set in the ISP/TSP Instruction Word.

MIP mapped

This indicates if the texture is MIP mapped.

VQ Compressed

This flag indicates that the texture uses 2x2 vector compression. Each 2x2 quartet of pixels is represented by an eight bit code which then references a 256 entry code book.

Pixel Format

This field determines the format of the pixels in the texture. These are defined as follows :-

Pixel Format	Hex Code	Description
1555	0	One bit alpha, 555 RGB. Alpha can be ignored.
565	1	Opaque 565
4444	2	4 bit alpha
YUV422	3	2Pixels per 32 bits.
Bump Map	4	MSB is S, LSB is R.
8888	5	
Reserved	6	
888	7	

Scan Order

If set, then the texture is in a *non-twiddled* format. *Twiddled* format is used to increase the efficiency of texture fetches from memory.

Stride Select

This flag is only relevant if the texture is in Scan Order. If set it indicates that the U (i.e. X) size of the texture is determined by a register setting (and the U-Size parameter is ignored). The value in that register is multiplied by 32.

Color Key Control

These bits control the color key test performed on the texture as shown below

MSB		LSB	
0	Enable	0	Use Color Key register 1
1	Disable	1	Use Color Key register 2

Multipass texture filtering

If this bit is set, then the hardware supports multipass texture filtering in order to achieve either linear interpolation between MIP Maps or tri-linear.

Palettised Texture

When set this bit determines that the texture is an 8bpp palletised texture.

Texture Address

Is the address of the base of the texture map. It is a 32 byte aligned address which implies a 64 MByte address space.

APPENDIX B. 3D REGISTERS

Writing to a 3D Register

The Access Register (Address 0xC0) has the following format:

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R/W		0001				Index (0x104) / Data (0x105)										H	I	Reserved			3D Register Address / Data											

R/W
00 Read
01 Write

Index/Data
0x104 when writing the 3D register index
0x105 when writing the 3D register data

H
Which half of a 32-bit register to read. (Always set to 1 for writes).
0 Read 16 LSBs
1 Read 16 MSBs

I
Auto increment.
1 Successive writes of data use incrementing addresses.

Writing to a 3D register involves the following steps:

Write the 3D Register Address to the Access Register using Index (0x104)
Optionally set auto increment
Write Register Data (16 bit LSBs) using Data (0x105)
Write Register Data (16 MSBs) using Data (0x105)
Optionally write more registers data (if auto increment)

Reading from a 3D Register

Write to the Access Register as described above to supply the register address to read. Autoincrementing is not supported for reads.

Read from the ReadAccess register (0xC8)

Note: When reading the ReadAccess register, the top 16 bits should be checked to ensure they match the top 16 bits written to the Access register. If not the register should be re-read. The bottom 16 bits returned is the data from the register.

3D Register Table

Index	Register	

Index	Register	
0014	STARTRENDER	R/W
0020	PARAM_BASE	R/W
002C	REGION_BASE	R/W
0030	SPAN_SORT_CFG	R/W
0040	INDEX_REF_ADDR	R/W
0044	LAT_COUNT	R/W
0048	FB_W_CTRL	R/W
004C	FB_W_LINESTRIDE	R/W
0050	INDEX_AGP_OFFSET	R/W
0054	INDEX_FB_OFFSET	R/W
005C	CBOOK_REF_ADDR	R/W
0060	CBOOK_AGP_OFFSET	R/W
0064	CBOOK_FB_OFFSET	R/W
0068	FB_X_CLIP	R/W
006C	FB_Y_CLIP	R/W
0074	FPU_SHAD_SCALE	R/W
0078	FPU_CULL_VAL	R/W
007C	FPU_PARAM_CFG	R/W
0080	HALF_OFFSET	R/W
0084	FPU_PERP_VAL	R/W
0088	ISP_BACKGND_D(L)	R/W
008C	ISP_BACKGND_T(H)	R/W
0098	ISP_FEED_CFG	R/W
00A4	FB_W_PRI_SOF	R/W
00B0	FOG_COL_RAM	R/W
00B4	FOG_COL_VERT	R/W
00B8	FOG_DENSITY	R/W
00BC	FOG_CLAMP_MAX	R/W
00C0	FOG_CLAMP_MIN	R/W
00E4	TEXT_CONTROL	R/W
00E8	ENDIAN_CTRL	R/W
00F4	SCALER_CTL	R/W
0118	Y_COEFF	R/W
0124	COLOUR_KEY1	R/W
0128	COLOUR_KEY2	R/W
0200 – 03FC	FOG_TABLE	R/W

STARTRENDER

Writing to this address causes 3D rendering to commence.

PARAM_BASE

bits 27 - 20 = ISP/TSP Parameter Base Address

bits 19 - 0 = 0x0

REGION_BASE

bits 27 - 2 = Region Base Address
bit 1 - 0 = 00

SPAN_SORT_CFG

bit 0 = Span sort enable
1: Enable
0: Disable

bit 8 = Offset Sort Enable
1: Enable
0: Disable

bit 16 = Cache Bypass
1: Bypass Cache
0: Use cache

INDEX_REF_ADDR

bits 7 - 0 = Ref address

Use is a as per **CBOOK_REF_ADDR** (see below)

LAT_COUNT

FB_W_CTRL

bits 2 - 0 = Pixel packing mode
000 - 555 16 bit RGB
001 - 565 RGB 16 bit
010 - 4444 ARGB 16 bit
011 - 1555 ARGB 16 bit
100 - 888 RGB 24 bit packed
101 - 888 RGB 32 bit
110 - 8888 ARGB 32 bit
111 - Reserved

bit 3 = fb_dither
'1' - dither 16bpp pixel modes
'0' – no dither

bits 15:8 = fb_kval

bits 23:16 = fb_alpha_threshold

FB_W_LINESTRIDE

bits 8:0 = Frame Buffer Line Stride

INDEX_AGP_OFFSET

bits 28 - 0 = 64 Bit Aligned physical base of GART.

INDEX_FB_OFFSET

bits 28 - 0 = 64 Bit Aligned physical base of frame buffer.

CBOOK_REF_ADDR

bits 7 - 0 = Ref address

If this value is less than the top 8 bits of the texture address used for a code book access then the code book accessed is made at the following address,

Addr = (TextAddr - RefAddr) + CBOOK_AGP_OFFSET.

This operation is addition to the GART boundary and base address.

CBOOK_AGP_OFFSET

bits 28 - 0 = 64 Bit Aligned physical base of GART.

CBOOK_FB_OFFSET

bits 28 - 0 = 64 Bit Aligned physical base of frame buffer.

FB_X_CLIP

bits 10 - 0 = Frame Buffer x clipping min
bits 26 - 16 = Frame Buffer x clipping max

FB_Y_CLIP

bits 10 - 0 = Frame Buffer y clipping min
bits 26 - 16 = Frame Buffer y clipping max

FPU_SHAD_SCALE

bits 7 - 0 = Scale factor for shadows
bit 8 = Simple Shadow Enable

FPU_CULL_VAL

bits 30 - 0 = floating point value for culling compare

FPU_PARAM_CFG

bits 3 - 0 = pointer first burst size
bits 7 - 4 = pointer burst size
bit 13 - 8 = ISP parameter burst trigger threshold
bit 19 - 14 = TSP parameter burst trigger threshold
bit 20 = Reserved

HALF_OFFSET

bit 0 = FPU pixel sampling position
bit 1 = TSP pixel sampling position
bit 2 = TSP texel sampling position

FPU_PERP_VAL

bits 30 - 0 = floating point value for perpendicular triangle compare

ISP_BACKGND_D(L)

bits 31 - 4 = Background Plane depth parameter

ISP_BACKGND_T(H)

Background plane tag parameter

bit 28 = cache hint
bit 27 = shadow parameters present
bits 26 - 24 = skip
bits 23 - 3 = tag address
bits 2 - 0 = tag offset

ISP_FEED_CFG

bit 0 = pre-sort mode
bit 1 = z sort
bit 2 = reverse sort

FB_W_PRI_SOF

bits 28 - 0 = w_sof_addr
bits 30 - 29 = write_priority

FOG_COL_RAM

bits 23 - 16 = TSP fog colour - fog table fogging - Res
bits 15 - 8 = TSP fog colour - fog table fogging - Green
bits 7 - 0 = TSP fog colour - fog table fogging - Blue

FOG_COL_VERT

bits 23 - 16 = TSP fog colour - per vertex fogging - Red
bits 15 - 8 = TSP fog colour - per vertex fogging - Green
bits 7 - 0 = TSP fog colour - per vertex fogging - Blue

FOG_DENSITY

bits 15 - 0 = TSP fog multiplication value

FOG_CLAMP_MAX

bits 31 - 24 = TSP pre-fog clamp colour - maximum value Alpha
bits 23 - 16 = TSP pre-fog clamp colour - maximum value Red
bits 15 - 8 = TSP pre-fog clamp colour - maximum value Green
bits 7 - 0 = TSP pre-fog clamp colour - maximum value Blue

FOG_CLAMP_MIN

bits 31 - 24 = TSP pre-fog clamp colour - minimum value Alpha
bits 23 - 16 = TSP pre-fog clamp colour - minimum value Red
bits 15 - 8 = TSP pre-fog clamp colour - minimum value Green
bits 7 - 0 = TSP pre-fog clamp colour - minimum value Blue

FOG_TABLE (0x0200 – 0x03FD)

bits 15 - 0 : Fog table Data

TEXT_CONTROL

bits 5 - 0 = stride
bits 12 - 8 = bank bit

ENDIAN_CTRL

bits 1- 0 = Index endian control
bits 2- 3 = Code book/normal texture endian control.

Endian control value

00 : No swap
01 : Swap 16 bit words
10 : Swap bytes within 16 bit words
11 : Swap bytes.

SCALER_CTL

bits 15 - 0 = Vertical scale factor
bit 16 = Horizontal scaling enable
bit 17 = Interlace on /off
bit 18 = Field Select

Y_COEFF

Filter coefficients for down scaling

bits 7 - 0 = Coefficient 0/2
bits 15 - 8 = Coefficient 1

COLOUR_KEY1

bits 23 - 16 = Red
bits15 - 8 = Green
bits 7 - 0 = Blue

COLOUR_KEY2

bits 23 - 16 = Red
bits15 - 8 = Green
bits 7 - 0 = Blue

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[0]More info please. Also for 1B target should be no resistors required...